

MP0107

09/348,865

PATENT

**IN THE CLAIMS**

Following is a complete and revised listing of the claims, marked with status identifiers in parentheses, underlines indicating insertions, and strikethroughs or double-brackets indicating deletions. This listing is to replace all prior listings of the claims.

1. (Previously Presented) A data network comprising:  
  
at least one crossbar, wherein each crossbar comprises N ports;  
  
a plurality N of devices each associated with and connected to one port of one of said crossbars;  
  
wherein each one port of one crossbar comprises:  
  
an input buffer for receiving messages from the device connected to its port and for sending said messages to the N-1 other ports of said one crossbar;  
  
a plurality N-1 of port output buffers, each corresponding to one of said N-1 other ports, wherein each of said plurality of N-1 of port output buffers receives said messages only from a corresponding input buffer corresponding to one of said N-1 other ports;  
  
a plurality N-1 of fullness sensors, each associated with one port output buffer, for measuring the fullness state of its associated port output buffer;  
  
shutoff means, connected to the fullness sensors associated with the port output buffers corresponding to said one port at said N-1 other ports, for, when said fullness state for one of said other ports is generally full, indicating to said device connected to said one port not to send data for the port which is now generally full.
2. (Previously Presented) A data network comprising:  
  
at least one crossbar, wherein each crossbar comprises N ports;

MP0107

09/348,865

PATENT

a plurality N of devices each associated with and connected to one port of one of said crossbars;

wherein each one port of one crossbar comprises:

an input buffer for receiving messages from the device connected to its port and for sending said messages to the N-1 other ports of said one crossbar;

a plurality N-1 of port output buffers, each corresponding to one of said N-1 other ports, wherein each of said plurality of N-1 of port output buffers receives said messages only from a corresponding input buffer corresponding to one of said N-1 other ports;

a plurality N-1 of fullness sensors, each associated with one port output buffer, for measuring the fullness state of its associated port output buffer;

shutoff means, connected to the fullness sensors associated with the port output buffers corresponding to said one port at said N-1 other ports, for, when said fullness state for one of said other ports is generally full, indicating to said device connected to said one port not to send data for the port which is now generally full,

wherein each device additionally comprises N-1 device output buffers, one per the N-1 other ports of said crossbar.

3. (Original) A network according to claim 2 and wherein each device also comprises a multiplicity of direct memory access (DMA) units for removing data from at least one of said device output buffers.

4. (Original) A network according to claim 1 and wherein each crossbar comprises an arbiter for providing said messages from said N-1 port output buffers to said device connected to its port only if said device is not full.

MP0107

09/348,865

PATENT

5. (Previously Presented) A network according to any of the preceding claims 1-4, and wherein each port comprises a bus link connected to said corresponding associated device.

6. (Cancelled)

7. (Previously Presented) A crossbar for communicating with at least one device, said crossbar comprising:

N ports, each one of said N ports comprising:

a link logic unit to receive messages and data from a respective device,

an input buffer to store data from the respective device,

N-1 output buffers each corresponding to another one of said N-1 ports;

and

a port arbiter to select one of said N-1 output buffers to output data to the respective device,

wherein said input buffer transfers the stored data to the corresponding output buffer of a selected one of the other one of said N ports.

8. (Previously Presented) A crossbar according to Claim 7, wherein said link logic unit determines a type of message from the respective device.

9. (Previously Presented) A crossbar according to Claim 8, wherein if the type of message is a local link message, a port function is performed and the message is not transferred.

MP0107

09/348,865

PATENT

10. (Previously Presented) A crossbar according to Claim 8, wherein if the type of message is a switch link message, the message and the data are transferred.

11. (Previously Presented) A crossbar according to Claim 7, wherein said device comprises one of a switch and a second crossbar.

12. (Previously Presented) A crossbar according to Claim 11, wherein said N-1 output buffers comprises a device table register to store a device number if the device comprises the switch.

13. (Previously Presented) A crossbar according to Claim 11, wherein said N-1 output buffers comprises a device table register to store device numbers of devices connected to the second crossbar.

14. (Previously Presented) A crossbar according to Claim 7,  
wherein if the device is unable to receive data, the device provides a message to said link logic unit, and

wherein said link logic unit signals said arbiter to inhibit communication to the device.

15. (Previously Presented) A crossbar according to Claim 7,  
wherein if an  $n^{\text{th}}$  one of said of said N-1 output buffers is at least a predetermined capacity, a signal is sent to the  $n^{\text{th}}$  one of said port arbiter of the other one of said N-1 ports to inhibit further transmission.

MP0107

09/348,865

PATENT

16. (Previously Presented) A network switch in communication with one port of a crossbar having N ports, said network switch comprising:

N-1 output buffers, each corresponding to N-1 other ports of the N ports of the crossbar, each of said N-1 output buffers comprising:

a direct memory access unit, and

a FIFO; and

an arbiter for controlling communications between said N-1 output buffers and the crossbar,

wherein when the crossbar signals said arbiter to inhibit sending data to an  $n^{\text{th}}$  one of the N-1 other ports, an  $n^{\text{th}}$  direct memory access unit stops transferring data from an  $n^{\text{th}}$  FIFO while other ones of said N-1 direct memory access units are not inhibited from transferring data.

17. (Previously Presented) A network apparatus comprising:

a crossbar for communicating with at least one device, said crossbar comprising:

N ports, each one of said N ports comprising:

a link logic unit to receive messages and data from a respective device,

an input buffer to store data from the respective device,

N-1 output buffers each corresponding to another one of said N-1 ports;

and

a port arbiter to select one of said N-1 output buffers to output data to the respective device,

wherein said input buffer transfers the stored data to the corresponding output buffer of a selected one of the other one of said N ports,

wherein said at least one device comprises:

MP0107

09/348,865

PATENT

a network switch in communication with an  $m^{\text{th}}$  port of said crossbar, said network switch comprising:

N-1 output buffers, each corresponding to N-1 other ports of the N ports of said crossbar, each of said N-1 output buffers comprising:

a direct memory access unit, and

a FIFO; and

an arbiter in communication with said port arbiter for controlling communications between said N-1 output buffers and the crossbar,

wherein when said crossbar signals said arbiter to inhibit sending data to an  $n^{\text{th}}$  one of said N-1 other ports, an  $n^{\text{th}}$  direct memory access unit stops transferring data from an  $n^{\text{th}}$  FIFO while other ones of said N-1 direct memory access units are not inhibited from transferring data.

18. (Previously Presented) A crossbar for communicating with at least one device, said crossbar comprising:

N port means, each one of said N port means comprising:

link logic means for receiving messages and data from a respective device,

input buffer means for storing data from the respective device,

N-1 output buffer means each corresponding to another one of said N-1 port means; and

port arbiter means for selecting one of said N-1 output buffer means for outputting data to the respective device,

wherein said input buffer means transfers the stored data to the corresponding output buffer means of a selected one of the other one of said N port means.

MP0107

09/348,865

PATENT

19. (Previously Presented) A crossbar according to Claim 18, wherein said link logic means determines a type of message from the respective device.

20. (Previously Presented) A crossbar according to Claim 19, wherein if the type of message is a local link message, a port function is performed and the message is not transferred.

21. (Previously Presented) A crossbar according to Claim 19, wherein if the type of message is a switch link message, the message and the data are transferred.

22. (Previously Presented) A crossbar according to Claim 18, wherein said device comprises one of a switch and a second crossbar.

23. (Previously Presented) A crossbar according to Claim 22, wherein said N-1 output buffer means comprises a device table register means for storing a device number if the device comprises the switch.

24. (Previously Presented) A crossbar according to Claim 22, wherein said N-1 output buffer means comprises a device table register means for storing device numbers of devices connected to the second crossbar.

25. (Previously Presented) A crossbar according to Claim 18,  
wherein if the device is unable to receive data, the device provides a message to said link logic means, and

MP0107

09/348,865

PATENT

wherein said link logic means signals said arbiter means to inhibit communication to the device.

26. (Previously Presented) A crossbar according to Claim 18,

wherein if an  $n^{\text{th}}$  one of said of said N-1 output buffer means is at least a predetermined capacity, a signal is sent to the  $n^{\text{th}}$  one of said port arbiter means of the other one of said N-1 port means to inhibit further transmission.

27. (Previously Presented) A network switch in communication with one port of a crossbar having N port means, said network switch comprising:

N-1 output buffer means, each corresponding to N-1 other port means of the N port means of the crossbar, each of said N-1 output buffer means comprising:

direct memory access means for controlling memory access, and

FIFO buffer means for storing data; and

arbiter means for controlling communications between said N-1 output buffer means and the crossbar,

wherein when the crossbar signals said arbiter means to inhibit sending data to an  $n^{\text{th}}$  one of the N-1 other port means, an  $n^{\text{th}}$  direct memory access means stops transferring data from an  $n^{\text{th}}$  FIFO buffer means while other ones of said N-1 direct memory access means are not inhibited from transferring data.

28. (Previously Presented) A network apparatus comprising:

crossbar means for communicating with at least one device, said crossbar means comprising:

N port means, each one of said N port means comprising:



MP0107

09/348,865

PATENT

link logic means for receiving messages and data from a respective device,

input buffer means for storing data from the respective device,

N-1 output buffer means each corresponding to another one of said N-1 port means; and

port arbiter means for selecting one of said N-1 output buffer means to output data to the respective device,

wherein said input buffer means transfers the stored data to the corresponding output buffer means of a selected one of the other one of said N port means,

wherein said at least one device comprises:

network switch means for communicating with an  $m^{\text{th}}$  port of said crossbar, said network switch means comprising:

N-1 output buffer means, each corresponding to N-1 other port means of the N port means of said crossbar means, each of said N-1 output buffer means comprising:

direct memory access means, and

FIFO buffer means; and

arbiter means in communication with said port arbiter for controlling communications between said N-1 output buffer means and the crossbar,

wherein when said crossbar signals said arbiter means to inhibit sending data to an  $n^{\text{th}}$  one of said N-1 other port means, an  $n^{\text{th}}$  direct memory access means stops transferring data from an  $n^{\text{th}}$  FIFO BUFFER MEANS while other ones of said N-1 direct memory access means are not inhibited from transferring data.